IN THE SPECIFICATION

Please amend the specification as follows where marked-up versions of the changed paragraphs are attached as Appendix B:

Page 1, before the first paragraph, please insert:

Cross Reference to Related Applications

This is a continuation of prior application serial no. 09/348,958 filed July 7, 1999, now pending.

Delete the paragraph on page 2, between lines 29-30 of the specification.

~~By repeating pattern is meant a pattern (of 1's and 0's) indicating which bits within a respective data block are to be repeated.~~

Replace the paragraph on page 2, between lines 10-12 of the specification with the following:

In accordance with the present invention, the interleaving circuit does not need to be adaptive, because it is selected for interface with a coding circuit having a fixed code rate or a limited number of rates for a variable rate data source. The

puncturing circuit or repeating circuit then operates on the interleaved words in order to adjust the output bit rate to be appropriate for transmission over the transmission channel. The deletion or repetition pattern is then selected in such a way that (i) in the case of deletion of bits, the puncturing has ~~least at~~ the least detrimental effect to the digital circuit) which has been coded and interleaved before input to the puncturing circuit or (ii) in the case of repetition of bits, the repetition has the most beneficial effect for the output for transmission and is not concentrated at one portion of the digital input.

Replace the paragraph on page 7, between lines 23-31 of the specification with the following:

The channel coding circuit 14, 24 applies convolutional coding to the input data stream and generates a bit stream having a greater number of bits. In the example shown in Figure 2, the convolutional coding circuit converts a data stream of length k to a stream of length n, as shown in Figure 2 part B, which effectively increases the number of bits for transmission by n/k. Interleaving is applied to the coded data words and in the example shown in Figure 2 the inter-frame interleaving circuit 16 operates on 8-bit words from the coded data stream and applies a block interleaving algorithm with a depth of 4. Thus, the interleaving circuit bitwise fills an

interleaving matrix of 4 columns and 8 rows, row by row.

Replace the paragraph spanning pages 8-9, between page 8, line 24, and page 9, line 2 of the specification with the following:

Consequently, in the deletion/repetition pattern shown in Figure 2 part D the bits for deletion or repetition have been selected with a maximum of one such bit on each row of the interleaving matrix. By repetition pattern is meant a pattern (of 1's and 0's) indicating which bits within a respective data block are to be repeated. In the particular example shown in Figure 2, the deletion pattern for each interleaved word 44a, 44b, 44c, 44d is offset with respect to the adjacent interleaved word or words within the block. For example, interleaved word 44a has a deletion/repetition pattern of (10000100) applied to it, whereas interleaved word 44b has a deletion/repetition pattern of (01000010) applied to it, and so on. By offsetting the pattern in adjacent columns the problem of deleting or repeating adjacent bits is avoided and the pattern is straightforward to implement.